

CLAIMS

What is claimed is:

- 5 1. An integrated circuit comprising:
 - a body bias distribution circuit;
 - a pad coupled to said body bias distribution circuit, said pad for receiving an externally applied voltage;
 - an internal voltage bus; and
- 10 a circuit component coupled to said internal voltage bus and coupled to said body bias distribution circuit, wherein said internal voltage bus supplies a body bias voltage to said distribution circuit absent a voltage applied to said pad.
- 15 2. An integrated circuit as described in Claim 1 wherein said externally applied voltage is substantially applied to said distribution circuit when said externally applied voltage is applied to said pad.
- 20 3. An integrated circuit as described in Claim 2 wherein said circuit component is a resistor element.

4. An integrated circuit as described in Claim 2 further comprising an external pin coupled to said pad, said external pin for coupling with said externally supplied voltage.

5 5. An integrated circuit as described in Claim 2 wherein said internal voltage bus is coupled to a power supply voltage of said integrated circuit.

10 6. An integrated circuit as described in Claim 1 further comprising a plurality of metal oxide semiconductor transistors coupled to said body bias distribution circuit.

15 7. An integrated circuit as described in Claim 6 wherein said plurality of metal oxide semiconductor transistors are coupled to said distribution circuit via respective body terminals.

20 8. An integrated circuit device comprising a resistive structure disposed thereon for selectively coupling between a body bias voltage and a power supply voltage to body biasing wells.

9. The integrated circuit device of Claim 8 wherein said body bias voltage is externally supplied.

10. The integrated circuit device of Claim 8 wherein said power supply voltage is internally obtained.

11. The integrated circuit device of Claim 8 wherein said resistive
5 structure comprises n well and deep n well regions.

12. The integrated circuit device of Claim 8 wherein said resistive structure comprises p well and deep n well regions.

10 13. The integrated circuit device of Claim 8 wherein said resistive structure comprises a resistance of about 1 kilo ohm.

14. The integrated circuit device of Claim 8 wherein said coupling comprises a body bias distribution network comprising deep wells.

15 15. A semiconductor device comprising a first terminal for coupling a voltage to a body terminal of a metal oxide semiconductor, wherein said body terminal is not coupled to a source or a drain of said metal oxide semiconductor.

20 16. The semiconductor device of Claim 15 wherein said first terminal is a package pin of a semiconductor package.

17. The semiconductor device of Claim 15 wherein said first terminal
is a pad of an integrated circuit.

18. The semiconductor device of Claim 15 wherein said first terminal
5 is a coupling to a metal layer of said semiconductor device.

19. The semiconductor device of Claim 15 wherein said metal oxide
semiconductor operates as a digital device.

10 20. The semiconductor device of Claim 15 wherein said semiconductor
device comprises a microprocessor.

15 21. The semiconductor device of Claim 15 comprising a plurality of
metal oxide semiconductors.

22. A semiconductor device comprising:
a metal voltage rail coupled to a supply voltage;
a first region of n well diffusion disposed beneath and coupled to
said metal voltage rail; and

20 a second region of n well diffusion coupled to a plurality of n well
diffusion lines, wherein said n well diffusion lines couple a voltage of said
second region of n well diffusion to n well regions of semiconductor
devices;

wherein said first region of n well diffusion is coupled to said second region of n well diffusion; and

wherein further said first region of n well diffusion forms a predetermined resistance between said metal voltage rail and said second 5 region of n well diffusion.

23. The semiconductor device of Claim 21 wherein said predetermined resistance is about 1 kilo ohm.

10 24. The semiconductor device of Claim 21 for producing an n well body bias voltage that is different from a supply voltage.

15 25. The semiconductor device of Claim 21 wherein the resistance of said second region of n well diffusion is substantially less than the resistance of said first region of n well diffusion.

26. The semiconductor device of Claim 21 wherein the length of said first region of n well diffusion is substantially different from the width of said first region of n well diffusion.

20 27. The semiconductor device of Claim 21 wherein said second region of n well diffusion is substantially square.

28. The semiconductor device of Claim 21 wherein said supply voltage
is an operating voltage for semiconductor devices operated with a body bias.

29. A semiconductor device comprising:
5 a metal voltage rail coupled to a low supply voltage;
 a deep n well diffusion region coupled to said metal voltage rail;

and

an n well diffusion region surrounding a portion of said deep n well
diffusion region to isolate said portion of said deep n well diffusion region
10 from a substrate;

wherein said deep n well diffusion region is coupled to said
substrate; and

wherein further said deep n well diffusion region forms a
predetermined resistance between said metal voltage rail and said
15 substrate.

30. The semiconductor device of Claim 29 wherein said predetermined
resistance is about 1 kilo ohm.

20 31. The semiconductor device of Claim 29 wherein said low supply
voltage is substantially ground.

32. The semiconductor device of Claim 29 for producing an n well body bias voltage that is different from a ground voltage.

33. The semiconductor device of Claim 29 wherein the length of said
5 region of deep n well diffusion is substantially different from the width of said region of deep n well diffusion.

34. The semiconductor device of Claim 29 wherein said low supply voltage is a ground voltage for semiconductor devices operated with a body bias.

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35. A method of providing a body bias voltage in a semiconductor device comprising:

responsive to a coupling of an external body bias voltage to said semiconductor device, coupling said body bias voltage to body biasing wells of said semiconductor device; and

15 responsive to an absence of said external body bias voltage, automatically supplying said body biasing wells of said semiconductor device with an internal voltage of said semiconductor device through a resistance.

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36. The method of Claim 35 wherein said internal voltage is a power supply voltage for said semiconductor device.

37. The method of Claim 35 wherein said internal voltage is a ground reference for said semiconductor device.

38. The method of Claim 35 wherein said resistive structure comprises
5 an n well region.

39. The method of Claim 35 wherein said resistive structure forms a desired resistance between said internal voltage and said n well channels.

10 40. The method of Claim 39 wherein said desired resistance is about 1 kilo ohm.

41. The method of Claim 35 wherein said resistance is at least about one hundred times as large as a resistance of said coupling of said body bias
15 voltage to said body biasing wells of said semiconductor device.